

The diagram illustrates a packet processing system architecture. On the left, an **OIC** (103) receives multiple input streams (101, 102) and outputs to a series of **Ingress CDR** (106) blocks. These connect to a **68 x 68 XBAR A** (105). The output of XBAR A goes through an **LPC** (104) block to a **68 x 68 XBAR B** (107). Between the two XBARs is a **PMM** (108) block. The output of XBAR B connects to **Egress CDR** blocks (111, 112), which then connect to **SFC X** (109) and **SFC Y** (110). A **Processor Module** (113) is connected to the OIC and the Egress CDRs. A dashed box encloses the Ingress CDRs, XBAR A, LPC, PMM, XBAR B, and Egress CDRs.

Figure 1

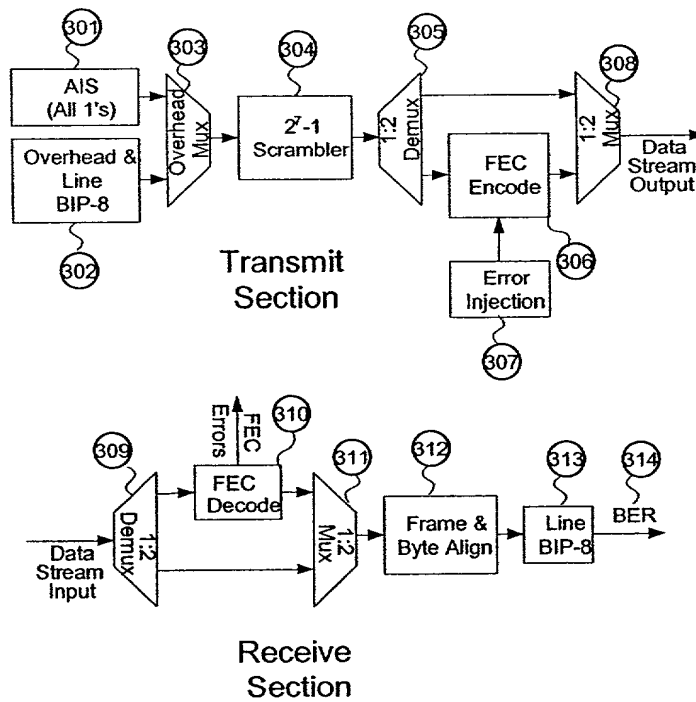


Figure 3:

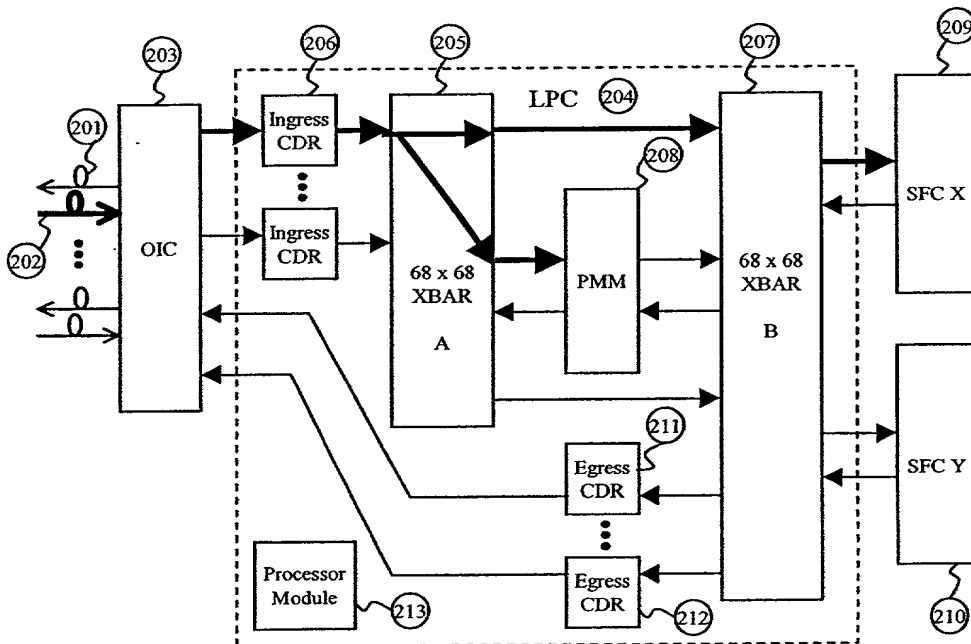


Figure 2:

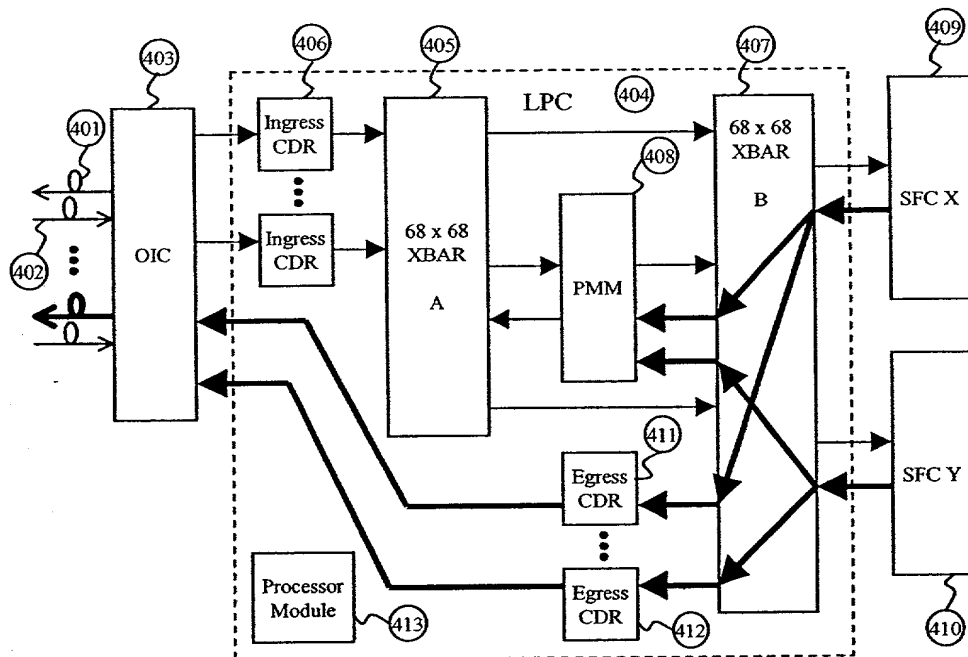


Figure 4:

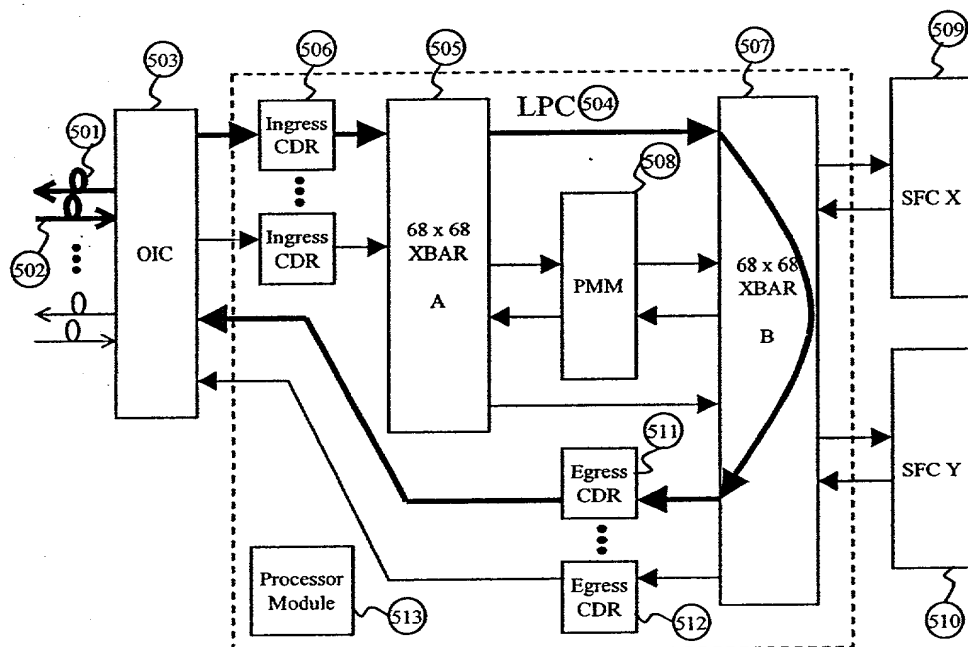


Figure 5:

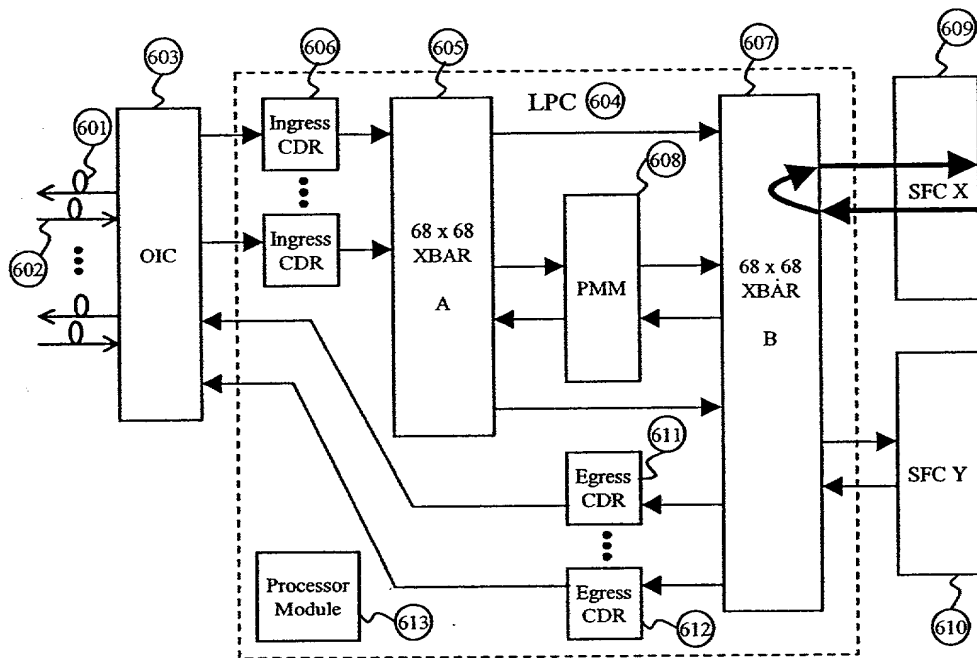


Figure 6: